CONFIGURABLE ELECTRONIC CIRCUIT, IN PARTICULAR ONE DEDICATED TO ARITHMETIC CALCULATIONS

Field of the Invention

[0001]　　The present invention relates to configurable electronic circuits, and in particular, but not limited to, those dedicated to arithmetic calculations.

Background of the Invention

[0002]　　Conventional configurable circuits include Field Programmable Gate Array (FPGA) circuits marketed by the company Xilinx. These circuits are made up of look-up tables or memories that can be programmed independently, and interconnection elements that are also programmable. The look-up tables have a fine programming granularity, generally to the bit level, and can be used to implement conventional logic functions such as OR and AND functions, for example, with two or three inputs.

[0003]　　When implementing a multiplier with such circuits, the result is a circuit having a large surface area. Families of products marketed by Xilinx, such as the products of the Virtex family, do indeed incorporate multipliers, for example, 18 x 18 bit multipliers. However, the designer is faced with some inflexibility in programming these multipliers, since it is difficult to produce, from these 18 x 18 bit multipliers, 8 x 8 bit multipliers or 32 x 32 bit multipliers, for example.

Summary of the Invention

[0004]   An object of the present invention is to provide an electronic circuit that is configurable and exhibits a high degree of programming flexibility.   In particular, the circuit may be dedicated to arithmetic calculations, such as the types of calculations performed in baseband processors incorporated in cellular mobile telephones, for example.   The circuit may be produced before the arithmetic and/or logic functions are known, wherein these functions will actually be executed in the application being considered.

[0005]   Another object of the present invention is to provide such a circuit that is programmable at the bit level while having a reasonable size.

[0006]   The reconfigurable electronic circuit according to the present invention includes at least one tile or building block circuit.   This tile comprises at least two individual cells interconnected.

[0007]   Each individual cell may comprise the following: a multiplier; an arithmetic and logic unit for performing at least one arithmetic and/or logic function that can be selected from a predetermined set of arithmetic and/or logic functions; a vertical bus; a first configurable switching block connected to the vertical bus and to the inputs of the multiplier; second configurable switching means or circuit connected to the vertical bus and to the output of the multiplier; and a third configurable switching means or circuit connected to the vertical bus and to the output of the multiplier of the other individual cell.

[0008]   Each cell may further comprise the following: a second configurable switching block connected to the

vertical bus and to the inputs of the arithmetic and logic unit; fourth configurable switching means or circuit connected to the vertical bus and to the output of the arithmetic and logic unit; a carry propagation bus linking the two arithmetic and logic units of the individual cells; a terminal switching block that is configurable and connected to the vertical bus; and a horizontal bus linking the two terminal switching blocks of the two individual cells.

[0009] The configurable nature of the tile arises in particular from the configurable nature of the arithmetic and logic units with respect to the arithmetic and/or logic functions that can be selected (configured) from a set of possible predetermined functions, and from the configurable nature of the switching (interconnection) blocks and circuit. This implies that some or all of the bits of the words conveyed over the horizontal and vertical buses can be selected, so as to be able to, on command, either switch them to one or the other of the two individual cells or perform arithmetic, logic or multiplication operations with a variable number of bits.

[00010] Control means or a control circuit is assigned to the tile to deliver configuration signals for configuring the various registers and elements of the arithmetic and logic units, multipliers and the switching circuits and blocks. According to one embodiment, each multiplier may be an m x n bit multiplier having two inputs intended to receive two words of m and n bits respectively, and an output intended to deliver an output word of m + n bits.

[00011] The second switching means or circuit of a first individual cell of the tile is then intended to

receive n lower order bits of the output word delivered
by the multiplier of the first cell, while the third
switching means or circuit of this first individual
cell is intended to receive n lower order bits of the
output word delivered by the multiplier of the second
individual cell of the tile.

[00012]   Furthermore, the second switching means or
circuit of the second individual cell is intended to
receive m higher order bits of the output word
delivered by the multiplier of this second cell, while
the third switching means or circuit of this second
individual cell is intended to receive m higher order
bits of the output word delivered by the multiplier of
the first individual cell.

[00013]   Thus, when carrying out, for example, a
complex multiplication of a first complex number $a_r + ja_i$
by a second complex number $b_r + jb_i$, a tile will execute
the partial products $a_r * b_r$ and $a_i * b_i$. If it is assumed
that a_r, a_i is coded with n bits and b_r, b_i is coded
with m bits, the vertical bus of a first individual
cell conveys to the output of the multiplier the 2n
lower order bits of the result of the multiplication,
that is, the n lower order bits of the product $a_r * b_r$ and
the n lower order bits of the product $a_i * b_i$.

[00014]   Furthermore, the vertical bus of the other
individual cell conveys the 2m higher order bits, that
is, the m higher order bits of the product $a_r * b_r$ and the
m higher order bits of the product $a_i * b_i$. In such an
embodiment, each bus of the tile can, for example,
convey words having a number of bits at least equal to
the lowest common multiple (LCM) of m and n.

[00015]   According to one particularly straightforward
embodiment, m is equal to n. In this case, each bus of

the tile has, for example, p tracks of n bits, with p being an integer greater than 1. Thus, in one such embodiment, the configurable switching circuits and blocks can be configured to select particular tracks of the bus, so as, for example, to process words of n bits being conveyed on a particular track of a bus and to return the result of the operation on another track of the bus.

[00016]   To implement a configurable circuit having a larger structure with more calculation possibilities or one that is able to perform calculations on data having a greater number of bits, several tiles can be interconnected. Moreover, it is particularly advantageous that the tiles then be connected in quincunx form, which facilitates in particular the sequencing of the operations in the case of multiplications on high numbers of bits involving several tiles.

[00017]   According to one embodiment of the invention, the circuit additionally includes a sign extension module connected to two adjacent tiles of the same horizontal row. This sign extension module is connected between the arithmetic and logic unit of an individual cell of a first tile and the vertical bus of the individual cell of the second tile. This cell is immediately adjacent to the individual cell of the first tile.

[00018]   The presence of such an extension module means that sign extension can be implemented without using, in this respect, the arithmetic and logic unit. However, in certain applications, it may be possible to dispense with such a sign extension module and

implement this function in the arithmetic and logic unit.

[00019]   So that extended accumulation operations, in particular, can be implemented easily, it is especially advantageous that the tile also include an additional row of arithmetic and logic units. More specifically, such an additional row includes two vertical bus extensions connected to two terminal switching blocks respectively; two additional terminal switching blocks connected to the two vertical bus extensions respectively; one additional horizontal bus connected between the two additional terminal blocks; two additional arithmetic and logic units connected to the two vertical bus extensions respectively, via additional configurable switching circuits; and one additional carry propagation bus connected between the two additional arithmetic and logic units.

[00020]   Then, advantageously, provision is made for specific buses enabling long connections interlinking additional arithmetic and logic units of adjacent tiles of the same column. The configurable circuit according to the invention may be implemented in the form of an integrated circuit, for example.

Brief Description of the Drawings

[00021]   Other advantages and features of the invention will become apparent upon examination of the detailed description of entirely non-limiting embodiments, and of the accompanying drawings in which:

[00022]   Figure 1 shows schematically an embodiment of a tile according to the present invention;

[00023]   Figure 2 illustrates in greater detail one part of the tile of Figure 1 in a specific application;

[00024] Figures 3 to 7 shows schematically in greater detail certain parts of the tile according to the present invention;

[00025] Figure 8 illustrates one embodiment of a circuit according to the present invention having several tiles connected in a quincunx fashion;

[00026] Figures 9 and 10 show schematically an example operation that can be performed by a circuit according to the present invention; and

[00027] Figures 11 and 12 show schematically another example operation that can be performed by a circuit according to the present invention.

Detailed Description of the Preferred Embodiments

[00028] In Figure 1, the reference TL denotes a tile or building block circuit of a configurable circuit according to the invention. The illustrated tile TL is itself configurable and is made up of two individual cells CEL1 and CEL10 that are interconnected. The cell CEL1 has a terminal BE1, which may be an input terminal or an output terminal.

[00029] From this terminal BE1 extends a vertical bus BSV1 made up in this case of p tracks of n bits each, for example, 16 bits each. On this vertical bus BSV1, there is arranged a first configurable switching block, in this case made up of two individual switching circuits CBX1A and CBX1B.

[00030] The lateral outputs of these two individual switching circuits CBX1A and CBX1B are linked via two secondary buses to two inputs of a multiplier MX1, which is in this case an n x n bit multiplier. This multiplier MX1 delivers a 2n-bit output word (in this

particular case 32 bits) on an output bus which is split into two parts.

[00031] A first part of this bus, conveying in this case n bits, is connected to a second configurable switching circuit CBX2 also connected to the vertical bus BSV1. The second part of this output bus, also conveying n bits, is linked to a third configurable switching circuit CBX30 connected to the vertical bus BSV10 of the other individual cell of the tile, referenced CEL10.

[00032] The third configurable switching circuit CBX3 of the cell CEL1 is, for its part, connected both to the vertical bus BSV1 and to the output of the multiplier MX10 of the cell CEL10. This switching circuit CBX3 is intended to receive n bits of the output word delivered by the multiplier MX10, while the n remaining bits are delivered to the second configurable switching circuit CBX20 of the cell CEL10.

[00033] A second configurable switching block is in this case made up of two individual switching circuits CBX4A and CBX4B which are connected both to the vertical bus BSV1 and to the two inputs of an arithmetic and logic unit ALU1. A fourth configurable switching circuit CBX5 is connected to the vertical bus and to the output of the arithmetic and logic unit ALU1. Furthermore, a carry propagation bus BPR links the two arithmetic and logic units ALU1 and ALU10 of the two cells CEL1 and CEL10.

[00034] A configurable terminal switching block SBX1 is connected both to the vertical bus BSV1 and to a horizontal bus BH linking the two terminal switching blocks SBX1 and SBX10 of the two cells CEL1 and CEL10.

This horizontal bus BH is also, in this case, a bus made up of p tracks of n bits each.

[00035] For the case in which the tile TL does not include an additional row RS of arithmetic and logic units, such as that shown by the shaded area in Figure 1, the two terminal switching blocks SBX1 and SBX10 form two other input/output terminals of the tile TL. Of course, the switching circuits CBX10A, CBX10B, CBX40A, CBX40B and CBX50 are identical to the equivalent circuits of the cell CEL1.

[00036] Before returning in greater detail to the structure and functionality of the additional row RS of arithmetic and logic units, reference will now be made more particularly to Figure 2 to introduce a yet more general embodiment of the tile according to the invention. More specifically, according to Figure 2, the multipliers MX1 and MX10 of the two cells CEL1 and CEL10 of the tile TL are m x n bits multipliers, and consequently deliver m + n bit output words.

[00037] In this case, as illustrated in Figure 2, the n bits of the output word delivered by the multiplier MX1 are directed to the second switching circuit CBX2 while the remaining m bits are directed to the third switching circuit CBX30 of the cell CEL10.

[00038] Likewise, the n bits of the output word delivered by the multiplier MX10 are delivered to the third switching circuit CBX3 of the cell CEL1 while the remaining m bits are directed to the second switching circuit CBX20 of the cell CEL10. In this embodiment, each of the vertical buses BSV1 and BSV10 has a number of bits at least equal to the lowest common multiple of m and of n (LCM(m,n)).

[00039]   Reference will now be made more particularly to Figures 3 to 7 to describe in greater detail certain parts of the individual cells of the tile TL. Figure 3 schematically illustrates an embodiment of an arithmetic and logic unit ALU. Such a unit is conventional and has a structure that is known. More specifically, it includes in this case blocks BLL capable of performing predetermined arithmetic and/or logic functions. These blocks BLL can be configured by configuration signals CONF sent by controller MCM. During each application, the blocks BLL can be configured via these configuration signals to define the arithmetic and/or logic functions that will actually be carried out by the unit ALU.

[00040]   These blocks BLL each receive two bits a_i, b_i belonging to two input words received by the unit ALU. The n bits of the result r_i are, for example, stored in registers RGRS which in this case are pipeline registers intended to improve the speed-related performance of the tiles. This being the case, the storage of result bits in registers is not obligatory. Moreover, circuit RGRE can be used to store the possible carry resulting from operations performed by the blocks BLL. The final carry is transmitted on the carry propagation bus BPR. The circuit RGRE receives an initial carry, for example, equal to zero for an addition and equal to 1 for a subtraction.

[00041]   Figures 4 and 5 illustrate more precisely the structure of a terminal switching block such as, for example, the one referenced SBX1. This terminal block SBX, or crossbar, has as many individual interconnection circuits CSB as there are tracks p on the vertical and horizontal buses BSV, BH. In the

example of Figure 4, the number of tracks p is equal to 4, and each track is able to convey 16-bit words, for example.

[00042] Each individual interconnection circuit CSB is placed at the intersection between a track pBSV of the vertical bus BSV and the equivalent track pBH of the horizontal bus BH. Each individual interconnection circuit CSB is configurable in that a word from a track of one of the buses BSV or BH can be switched to the equivalent track of the same bus or of the orthogonal bus, and this is regardless of the direction of conveyance of the word.

[00043] In this respect, an individual interconnection circuit CSB may be, for example, the one illustrated schematically in Figure 5. In this case, an interconnection circuit includes six transistors T1-T6 connected in a diamond configuration. Each transistor is controlled at its gate so as to configure the switching thus achieved. Moreover, at two of the inputs/outputs, provision may be made, preferably, for pairs of amplifiers with tristate control BF1 and BF2 (buffers). These buffers reshape the signal at two interconnection stages, and the direction chosen depends on the direction of propagation of the signal (position of the source). Even then, the control signals of the transistor gates and of the tristate buffers are provided by the controller MCM.

[00044] Figure 6 schematically represents a switching circuit, such as one of the above referenced types CBX1A, for example. The left part of Figure 6 schematically shows this switching circuit, such as the one illustrated in Figure 1, for example.

[00045]   The right part of Figure 6 schematically shows an example internal architecture corresponding to this representation. Thus, the switching circuit CBX1 can be formed by a multiplexer with four inputs and one output, configurable via a configuration signal SEL also issued by the controller MCM. Thus, with the switching circuit CBX1, it is possible to select one of the tracks of the bus BSV1 to copy the word A being conveyed on this selected track to the output of the multiplexer.

[00046]   Figure 7 illustrates in greater detail another type of switching circuit, for example, of the type of the one referenced CBX2. Here too, in the same way as in Figure 6, the left part of Figure 7 is a schematic representation of this switching circuit, such as the one which features, for example, in Figure 1, while the right part illustrates an example embodiment thereof.

[00047]   More specifically, the switching circuit CBX2 has tristate inverter elements controlled by a configuration signal SEL also issued by the controller MCM. Thus, a word A arriving at the input of the switching circuit CBX2 can be switched, depending on the value of the signal SEL, to one of the tracks of the bus BSV1.

[00048]   While the tile TL illustrated in Figure 1 is for carrying out simple operations, such as 16 x 16 bit multiplications or 8 x 8 bit multiplications, for example, it is possible, by interconnecting several tiles TL, vertically and/or horizontally, to perform more complex operations, or for example, multiplications on a larger number of bits.

[00049]   Figure 8 illustrates a configurable circuit
in which the tiles (in this case four tiles are
represented) are connected in a quincunx form. Such a
quincunx-type connection facilitates the sequencing of
operations during multiplications on a large number of
bits as will be discussed in greater detail below.

[00050]   The tiles are quincunx-connected such that
the vertical bus of the individual right-hand cell (in
Figure 8) of the tile TL3 is connected, via the
terminal switching block (crossbar) to the vertical bus
of the individual left-hand cell of the tile TL1.
Likewise, the vertical bus of the individual left-hand
cell of the tile TL3 is connected via a crossbar to the
vertical bus of the individual right-hand cell of the
tile TL2.

[00051]   Furthermore, the tiles of the same horizontal
row (line) are interconnected via horizontal buses and
crossbars, and via carry propagation buses. In the
example shown here, it is assumed that the tiles TL
were not furnished with additional rows RS of
arithmetic and logic units.

[00052]   Moreover, the configurable circuit CRF
includes, between two tiles of a given row, sign
extension modules MES12, MES34 for performing the sign
extension function which may be necessary during
operations performed by the arithmetic and logic units.
The presence of these sign extension modules means that
the arithmetic and logic units need not perform this
function, and this moreover means that their processing
capability need not be reduced.

[00053]   Figure 9 shows an example implementation of a
32 x 32 bit multiplication performed in a 32 x 32 bit
multiplier implemented using four 16 x 16 bit

multipliers. More specifically, the multiplication to be performed is the multiplication A*B, where A and B are two 32-bit numbers each having 16 higher order bits Ah and Bh, and 16 lower order bits Al and Bl.

[00054] As indicated in Figure 9, the four multiplications carried out are the products Al*Bl, Al*Bh, Ah*Bl and Ah*Bh respectively. Two additions, labelled 1 and 2 in Figure 9, are used to obtain, together with these multiplications, the result of the multiplication on 64 bits.

[00055] The 32 x 32 bit multiplier for performing this multiplication is, for example, the one represented in Figure 10. In this figure, three tiles TL5, TL6, TL7 have been used. It has also been assumed that the number of tracks of the vertical and horizontal buses was 5 and the tracks were referenced p1-p5 respectively.

[00056] Figure 10 also shows the configuration of the various switching blocks and circuits. More specifically, for example, the bits Ah are delivered as input on the track p1 of the vertical bus of the individual left-hand cell of the tile TL5. The bits Bl are delivered as input on the track p4 of the left-hand cell of the tile TL5. The bits Al are delivered as input on the track p2 of the right-hand cell of the tile TL5. The bits Bh are delivered as input on the track p3 of the right-hand cell of the tile TL5.

[00057] The multiplier of the left-hand cell of the tile TL5 performs the product Ah*Bl while the multiplier of the right-hand cell of the tile TL5 performs the product Al*Bh. The output word of the multiplier of the left-hand cell of the tile TL5 is distributed on the track p3 of the vertical bus of the

left-hand cell, and on the track p4 of the vertical bus
of the right-hand cell of the tile TL5.

[00058]   The output word of the multiplier of the
right-hand cell of the tile TL5 is distributed on the
track p5 of the vertical bus of the left-hand cell of
the tile TL5 and on the track p1 of the vertical bus of
the right-hand cell of the tile TL5.

[00059]   The two arithmetic and logic units of the
tile TL5 perform the addition operation No. 1
(Figure 9) and as a result supply, on the track p2 of
the vertical bus of the left-hand cell of the tile TL5
and on the track p5 of the vertical bus of the right-
hand cell of the tile TL5, the result of the arithmetic
operation Al*Bh + Ah*Bl.

[00060]   In regards now to the configuration of the
two terminal switching blocks (crossbars) for
connecting the tile TL5 to the tiles TL6 and TL7, it
will be noted that: the track p1 of the vertical bus of
the left-hand cell of the tile TL5 is connected to the
track p1 of the vertical bus of the right-hand cell of
the tile TL7; the track p2 of the vertical bus of the
left-hand cell of the tile TL5 is connected to the
track p2 of the vertical bus of the right-hand cell of
the tile TL7; the tracks p3 and p5 of the vertical bus
of the left-hand cell of the tile TL5 are not connected
to any other track; the track p4 of the vertical bus of
the left-hand cell of the tile TL5 is connected, via
the track p4 of the horizontal bus, to the track p4 of
the vertical bus of the left-hand cell of the tile TL6;
the tracks p1 and p4 of the vertical bus of the right-
hand cell of the tile TL5 are not connected to any
other track; the track p2 of the vertical bus of the
right-hand cell of the tile TL5 is connected to the

track p2 of the vertical bus of the left-hand cell of
the tile TL6; the track p3 of the vertical bus of the
right-hand cell of the tile TL5 is connected, via the
track p3 of the horizontal bus, to the track p3 of the
vertical bus of the right-hand cell of the tile TL7;
and the track p5 of the vertical bus of the right-hand
cell of the tile TL5 is connected to the track p5 of
the vertical bus of the left-hand cell of the tile TL6.

[00061]   The multiplier of the right-hand cell of the
tile TL7 gives the product Ah*Bh, and the result is
distributed on the track p5 of the vertical bus of the
left-hand cell of the tile TL7 and on the track p4 of
the vertical bus of the right-hand cell of this same
tile TL7.

[00062]   The multiplier of the left-hand cell of the
tile TL6 gives the product Al*Bl and the result is
distributed on the track p3 of the vertical bus of the
left-hand cell of the tile TL6 and on the track p2 of
the vertical bus of the right-hand cell of this same
tile TL6.

[00063]   The three arithmetic and logic units of the
left-hand cell of the tile TL6 and of the two cells of
the tile TL7 perform the addition operation no. 2 in
Figure 9, with a sign extension EXTS indicated by the
dashed line in Figure 10. The sixteen least
significant bits of the result C are delivered to the
track p2 of the vertical bus of the right-hand cell of
the tile TL6.

[00064]   Bits 16 to 31 are delivered to the track p1
of the vertical bus of the left-hand cell of the tile
TL6. Bits 32 to 47 are delivered to the track p5 of
the vertical bus of the right-hand cell of the tile
TL7. Moreover, the remaining bits that are the most

significant bits, that is, bits 48 to 63, are delivered
to track p4 of the vertical bus of the left-hand cell
of the tile TL7.

[00065]   Let us now return to Figure 1 to describe in
greater detail the structure of the additional row RS
of arithmetic and logic units, which a tile TL may
include. The additional row RS has two vertical bus
extensions PBSV1 and PBSV10 connected to the two
terminal switching blocks SBX1 and SBX10 respectively.

[00066]   This row also has two additional terminal
switching blocks SBX1S and SBX10S connected to the two
vertical bus extensions PBSV1 and PBSV10 respectively.
These two additional switching terminal blocks are
interconnected via an additional horizontal bus BHS.

[00067]   Two additional arithmetic and logic units
ALU1S and ALU10S are connected, respectively, to the
two vertical bus extensions PBSV1 and PBSV10 via
additional switching circuits CBX6A, CBX6B, CBX7, and
CBX60A, CBX60B and CBX70. Finally, an additional carry
propagation bus BPRS is connected between the two
additional arithmetic and logic units ALU1S and ALU10S.

[00068]   As well as the circuits that have just been
described, provision is also made for specific buses
BSPL1, BSPL10 intended to interconnect the additional
arithmetic and logic units of adjacent tiles of a given
column. Such a connection, that can be referred to as a
long connection, as opposed to the local connections
made by the various switching circuits and blocks of
the tile, is more particularly illustrated in
Figure 11. Figure 11 shows several tiles TL1-TL9
connected in a quincunx form and each is furnished with
an additional row of arithmetic and logic units.

[00069]   These additional rows, together with the specific long-connection buses, can be used, for example, to perform very straightforward accumulation operations, or for example, filtering operations, such as the sequences of operations illustrated in Figure 12, for example. In this Figure 12, which represents operations performed for example during a filtering process, there are represented six multiplications 1 to 6, and four additions 7 to 11.

[00070]   As illustrated in Figure 11, multiplication no. 1 is performed in the multiplier of the left-hand cell of the tile TL1, while multiplication no. 2 is performed in the multiplier of the right-hand cell of the tile TL3.

[00071]   Addition no. 7 is performed in the left-hand additional arithmetic and logic unit of the additional row RS1 of the tile TL1 and the result is transmitted, via a long connection, to the right-hand additional arithmetic and logic unit of the row RS3 of the tile TL3.

[00072]   Multiplications no. 3 and no. 4 are performed, respectively, in the left-hand and right-hand multipliers of the tiles TL4 and TL6, while addition No. 8 is performed in the left-hand additional arithmetic and logic unit of the additional row RS4 of the tile TL4. The result of this addition is transmitted via a long-connection bus to the right-hand arithmetic and logic unit of the additional row RS3, which performs addition No. 10.

[00073]   Multiplications no. 5 and no. 6 are performed, respectively, in the left-hand multiplier of the tile TL7 and in the right-hand multiplier of the tile TL8, while addition no. 9 is performed in the

left-hand additional arithmetic and logic unit of the
additional row RS7 of the tile TL7.

[00074] The result of this addition is transmitted to
the right-hand additional arithmetic and logic unit of
the additional row RS6 of the tile TL6 via a long-
connection bus. This additional arithmetic and logic
unit which also receives the result of addition no. 10
performs addition no. 11 and supplies the final result
of the operations.

[00075] The configurable circuit according to the
invention can thus be used to implement a number of
basic operations, for example, those often used in
algorithms implemented within digital signal processors
(DSPs). Such operations are, for example, 16 x 32 bit
multiplications, 32 x 32 bit multiplications, 16 x 16
bit complex multiplications, infinite impulse response
filters, and radix 2 or radix 4 butterfly operations
used in direct or inverse Fourier data transform
calculations.

[00076] The configurable circuit according to the
invention also forms a configurable data path and it
can be modified and extended by connecting several
tiles so as to form a structure of variable size with
greater computational power or enabling processing of
data occupying a much higher number of bits.

[00077] Furthermore, the circuit according to the
invention is not limited to the embodiments that have
just been described but covers all variants thereof.
Thus, the terminal blocks of the tiles could be located
at terminals BE1 and BE10. Also, the order in the
arrangement of multipliers and arithmetic and logic
units on the buses could be reversed. The same applies
for the arrangement of the additional row RS which

could be connected at the upper part of the tile (in
Figure 1).